IN THE CLAIMS:

Claims 3, 4, 6-8, 10, 11, 13-15, and 17-21 have been amended as follows:

1. (Original) A method of writing new information subsequently to an end of previous information written in a track of a record medium having a pre-recorded signal along the track, the method comprising the steps of:

reading a part of the previous information including the end thereof to generate a read signal divided into a sequence of frames;

start generating of a write signal in synchronization with a phase of the last frame of the read signal at the end of the previous information to thereby write the new information continuously from the end of the previous information; and then

shifting a period of a frame of the write signal relative to a period of a synchronization signal contained in the pre-recorded signal, thereby gradually adjusting a phase of the frame of the write signal to a phase of the synchronization signal of the pre-recorded signal.

2. (Original) The method according to claim 1, wherein the reading of a part of the previous information is carried out in response to a read clock derived from the previous information, the generating of the write signal is carried out in response to a write clock derived from the pre-recorded signal, such that a number of the write clock is shifted relative to the period of the synchronization signal of the pre-recorded signal to thereby gradually adjust the phase of the frame of the write signal to the phase of the synchronization signal of the prerecorded signal.

3. (Currently Amended) An apparatus capable of writing new information subsequently to an end of previous information written in a track of a record medium embedded with a pre-recorded signal along the track, the apparatus comprising:

a phase-locked ~~peop~~ loop circuit that generates a read clock for reading of the previous information and a write clock for writing of the new information; and

a control circuit that controls the phase-locked ~~peop~~ loop circuit to effect smooth continuation from the previous information to the new information, wherein the phase-locked ~~peop~~ loop circuit comprises a VCO that oscillates to generate an oscillating clock, a first phase comparator for comparing a phase of a read signal derived from the previous information with a phase of a clock signal derived from the oscillating clock so as to control the VCO based on phase-comparison between the read signal and the clock signal to thereby constitute a first loop of generating the read clock phase-locked to the read signal, a second phase comparator for comparing a phase of a synchronization signal derived from the pre-recorded signal with a phase or a clock signal derived from the oscillating clock so as to control the VCO based on phase-comparison between the synchronization signal and the clock signal to thereby constitute a second loop of generating the write clock phase-locked to the synchronization signal, the first loop and the second loop being switchable with respect to the VCO while the VCO maintaining the same frequency of the oscillating clock, and wherein the control circuit operates before starting the writing of the new information subsequent to the end of the previous information, for controlling the phase-locked ~~peop~~ loop circuit to activate the first loop to conduct the reading of a part of the previous information including the end thereof in synchronization to the read clock generated by

the first loop, and then switching the phase-locked ~~peop~~ loop circuit to activate the second loop when the reading of the previous information reaches the end so as to conduct the writing of the new information in synchronization to the write clock generated by the second loop.

4. (Currently Amended) The apparatus according to claim 3, wherein the control circuit operates when switching the phase-locked ~~peop~~ loop circuit from the first loop of generating the read clock to the second loop of generating the write clock, for resetting a phase of the clock signal fed to the second phase comparator in matching with a phase of the synchronization signal derived from the pre-recorded signal.

5. (Original) The apparatus according to claim 3 further comprising a pair of amplifiers connected to respective outputs of the first loop of generating the read clock and the second loop of generating the write clock for balancing loop gains between the first loop and the second loop.

6. (Currently Amended) An apparatus capable of writing new information subsequently to an end of previous information written in a track of a record medium embedded with a pro-recorded signal along the track, the apparatus comprising:

a phase-locked ~~peop~~ loop circuit that generates a read clock for reading of the previous information and a write clock for writing of the new information, the phase-locked ~~peop~~ loop circuit comprising a VCO that oscillates to generate an oscillating clock, a first phase comparator for comparing a phase of a read signal derived from the previous information with a phase of a clock signal derived from the oscillating clock so as to control the VCO based on phase-comparison between the read signal and the clock signal to thereby constitute a first loop of generating the read clock phase-locked

to the read signal, a second phase comparator for comparing a phase of a synchronization signal derived from the pre-recorded signal with a phase of a clock signal derived from the oscillating clock so as to control the VCO based on phase-comparison between the synchronization signal and the clock signal to thereby constitute a second loop of generating the write clock phase-locked to the synchronization signal, the first loop and the second loop being switchable with respect to the VCO while the VCO maintaining the same frequency of the oscillating clock;

a detecting circuit that detects the phase of each frame of the read signal derived from the previous information;

a generating circuit that generates a write signal representative of the new information in synchronization to the oscillating clock generated from the VCO; and

a control circuit that operates before starting the writing of the new information subsequent to the end of the previous information for controlling the phase-locked ~~poop~~ loop circuit to activate the first loop to conduct the reading of a part of the previous information including the end thereof in synchronization to the read clock generated by the first loop, and then operates when the reading of the previous information reaches the end for controlling the generating circuit to generate the write signal in matching with the phase of the last frame of the read signal detected at the end of the previous information to thereby start the writing of the new information in continuation from the end of the previous information and for switching the phase-locked ~~poop~~ loop circuit to activate the second loop.

7. (Currently Amended) The apparatus according to claim 6, further comprising a divider for dividing the oscillating clock fed from the VCO by a variable division ratio to

produce the clock signal fed to the second phase comparator, a third phase comparator for comparing a phase of each frame of the write signal with a phase of the synchronization signal derived from the pre-recorded signal to determine a phase difference between the write signal and the synchronization signal, and an adjuster operative after the phase-locked ~~peop~~ loop circuit is switched from the first loop of generating the read Clock to the second loop of generating the write clock for adjusting the variable division ratio of the divider so as to gradually absorb the phase difference.

8. (Currently Amended) The apparatus according to claim 6, wherein the control circuit operates when switching the phase-locked ~~peop~~ loop circuit from the first loop of generating the read clock to the second loop of generating the write clock, for resetting a phase of the clock signal fed to the second phase comparator in matching with a phase of the synchronization signal derived from the pre-recorded signal.

9. (Original) The apparatus according to claim 6, further comprising a pair of amplifiers connected to respective outputs of the first loop of generating the read clock and the second loop of generating the write clock for balancing loop gains between the first loop and the second loop.

10. (Currently Amended) An apparatus capable of writing new information subsequently to an end of previous information written in a track of a record medium embedded with a pre-recorded signal along the track, the apparatus comprising:

a read phase-locked ~~peop~~ loop circuit that generates a read clock for reading of the previous information, the read phase-locked ~~peop~~ loop circuit Comprising a first VCO that oscillates to generate an oscillating clock, a first phase comparator for comparing a phase of a read signal derived from the previous information with a phase

or a clock signal derived from the oscillating clock so as to control the first VCO based on phase-comparison between the read signal and the clock signal to thereby generate the road clock phase-locked to the read signal;

a write phase-locked ~~peop~~ loop circuit that generates a write clock for writing of the new information, the write phase-locked ~~peop~~ loop circuit comprising a second VCO that oscillates to generate an oscillating clock, a second phase comparator for comparing a phase of the read clock generated by the read phase-locked ~~peop~~ loop circuit with a phase of a clock signal derived from the oscillating clock of the second VCO so as to control the second VCO based on phase-comparison between the read clock and the clock signal to thereby constitute a first loop of synchronizing the oscillating clock of the second VCO with the read clock, and a third phase comparator for comparing a phase of a synchronization signal derived from the pre-recorded signal with a phase of a clock signal derived from the oscillating clock of the second VCO so as to control the second VCO based on phase-comparison between the synchronization signal and the clock signal to thereby constitute a second loop of generating the write clock phase-locked to the synchronization signal, the first loop and the second loop of the write phase-locked ~~peop~~ loop circuit being switchable with respect to the second VCO while the second VCO maintaining the same frequency of the oscillating clock; and

a control circuit that operates before starting the writing of the new information subsequent to the end of the previous information, for controlling the read phase-locked ~~peop~~ loop circuit to conduct the reading of a part of the previous information including the end thereof in synchronization to the read clock generated by the read phase-

locked ~~peop~~ loop circuit while controlling the write phase-locked ~~peop~~ loop circuit to activate the first loop for synchronizing the oscillating clock of the second VCO with the read clock, and then switching the write phase-locked ~~peop~~ loop circuit to activate the second loop when the reading of the previous information reaches the end so as to conduct the writing of the new information in synchronization to the write clock generated by the second loop of the write phase-locked ~~peop~~ loop circuit.

11. (Currently Amended) The apparatus according to claim 10, wherein the control circuit operates when switching the write phase-locked ~~peop~~ loop circuit from the first loop of synchronizing the oscillating clock to the second loop of generating the write clock, for resetting a phase of the clock signal fed to the third phase comparator in matching with a phase of the synchronization signal derived from the pre-recorded signal.

12. (Original) The apparatus according to claim 10, further comprising a pair of amplifiers connected to respective outputs of the first loop of synchronizing the oscillating clock and the second loop of generating the write clock for balancing loop gains between the first loop and the second loop.

13. (Currently Amended) An apparatus capable of writing new information subsequently to an end of previous information written in a track of a record medium embedded with a pre-recorded signal along the track, the apparatus comprising:

a read phase-locked ~~peop~~ loop circuit that generates a read clock for reading of the previous information, the read phase-locked ~~peop~~ loop circuit comprising a first VCO that oscillates to generate an oscillating clock, a first phase comparator for comparing a phase of a read signal derived from the previous information with a phase

of a clock signal derived from the oscillating clock so as to control the first VCO based on phase-comparison between the read signal and the clock signal to thereby generate the read clock phase-locked to the read signal;

a write phase-locked ~~peop~~ loop circuit that generates a write clock for writing of the new information, the write phase-locked ~~peop~~ loop circuit comprising a second VCO that oscillates to generate an oscillating cloak, a second phase comparator for comparing a phase of the read clock generated by the read phase-locked ~~peop~~ loop circuit with a phase of a clock signal derived from the oscillating clock of the second VCO so as to control the second VCO based on phase-comparison between the read clock and the clock signal to thereby constitute a first loop of synchronizing the oscillating clock of the second VCO with the read clock, and a third phase comparator for comparing a phase of a synchronization signal derived from the pre-recorded signal with a phase of a clock signal derived from the oscillating clock of the second VCO so as to control the second VCO based on phase-comparison between the synchronization signal and the clock signal to thereby constitute a second loop of generating the write clock phase-locked to the synchronization signal, the first loop and the second loop of the write phase-locked ~~peop~~ loop circuit being switchable with respect to the second VCO while the second VCO maintaining the same frequency of the oscillating clock;

a detecting circuit that detects the phase of each frame of the read signal derived from the previous information;

a generating circuit that generates a write signal representative of the new information in synchronization to the oscillating clock generated from the second VCO; and

a control circuit that operates before starting the writing of the new information subsequent to the end of the previous information for controlling the read phase-locked ~~peep~~ loop circuit to conduct the reading of a part of the previous information including the end thereof in synchronization to the read clock generated by the read phase-locked ~~peep~~ loop circuit while controlling the write phase-locked ~~peep~~ loop circuit to activate the first loop for synchronizing the oscillating clock of the second VCO to the read clock, and then operates when the reading of the previous information reaches the end for controlling the generating circuit to generate the write signal in matching with the phase of the last frame of the read signal detected at the end of the previous information to thereby start the writing of the new information in continuation from the end of the previous information and for switching the write phase-locked ~~peep~~ loop circuit to activate the second loop of generating the write clock.

14. (Currently Amended) The apparatus according to claim 13, further comprising a divider for dividing the oscillating clock fed from the second VCO by a variable division ratio to produce the clock signal fed to the third phase comparator, a fourth phase comparator for comparing a phase of each frame of the write signal with a phase of the synchronization signal derived from the pre-recorded signal to determine a phase difference between the write signal and the synchronization signal, and an adjuster operative after the write phase-locked ~~peep~~ loop circuit is switched from the first loop of synchronizing the oscillating clock to the second loop of generating the write clock for

adjusting the variable division ratio of the divider so as to gradually absorb the phase difference.

15. (Currently Amended) The apparatus according to claim 13, wherein the control circuit operates when switching the write phase-locked ~~peop~~ loop circuit from the first loop of synchronizing the oscillating clock to the second loop of generating the write clock, for resetting a phase of the clock signal fed to the third phase comparator in matching with a phase of the synchronization signal derived from the pre-recorded signal.

16. (Original) The apparatus according to claim 13, further comprising a pair of amplifiers connected to respective outputs of the first loop of synchronizing the oscillating clock and the second loop of generating the write clock for balancing loop gains between the first loop and the second loop.

17. (Currently Amended) An apparatus capable of writing new information subsequently to an end of previous information written in a track of a record medium embedded with a pre-recorded signal along the track, the apparatus comprising:

a read phase-locked ~~peop~~ loop circuit that generates a read clock for reading of the previous information, the read phase-locked ~~peop~~ loop circuit comprising a first VCO that oscillates to generate an oscillating clock, a first phase comparator for comparing a phase of a read signal derived from the previous information with a phase of a clock signal derived from the oscillating clock so as to control the first VCO based on phase-comparison between the read signal and the clock signal to thereby generate the read clock phase-locked to the read signal;

a write phase-locked ~~peop~~ loop circuit that generates a write clock for writing of the new information, the write phase-locked ~~peop~~ loop circuit comprising a second VCO that oscillates to generate an oscillating clock, a selector for selecting one of a synchronization signal derived from the pre-recorded signal and a divisional signal frequency-divided from the read clock at the same frequency as the synchronization signal, and a second phase comparator for comparing a phase of the selected one of the synchronization signal and the divisional signal with a phase of a clock signal derived from the oscillating clock of the second VCO so as to control the second VCO based on phase-comparison between the selected signal and the clock signal to thereby generate the write clock phase-locked to the selected signal; and

a control circuit that operates before starting the writing of the new information subsequent to the end of the previous information, for controlling the read phase-locked ~~peop~~ loop circuit to conduct the reading of a part of the previous information including the end thereof in synchronization to the read clock generated by the read phase-locked ~~peop~~ loop circuit while controlling the selector of the write phase-locked ~~peop~~ loop circuit to select the divisional signal of the read clock for synchronizing the oscillating clock of the second VCO with the read clock, and then controlling the selector of the write phase-locked ~~peop~~ loop circuit to select the synchronization signal when the reading of the previous information reaches the end so as to conduct the writing of the new information in synchronization to the write clock generated by the write phase-locked ~~peop~~ loop circuit.

18. (Currently Amended) The apparatus according to claim 17, wherein the control circuit operates when switching the selector of the write phase-locked ~~peop~~ loop circuit

from the divisional signal of the read clock to the sync clock of the pre-recorded signal, for resetting a phase of the clock signal fed to the second phase comparator in matching with a phase of the synchronization signal derives from the pre-recorded signal.

19. (Currently Amended) An apparatus capable of writing new information subsequently to an end of previous information written in a track of a record medium embedded with a pre-recorded signal along the track, the apparatus comprising:

a read phase-locked ~~peep~~ loop circuit that generates a read clock for reading of the previous information, the read phase-locked ~~peep~~ loop circuit comprising a first VCO that oscillates to generate an oscillating clock, a first phase comparator for comparing a phase of a read signal derived from the previous information with a phase of a clock signal derived from the oscillating clock so as to control the first VCO based on phase-comparison between the read signal and the clock signal to thereby generate the read clock phase-locked to the read signal;

a write phase-locked ~~peep~~ loop circuit that generates a write clock for writing of the new information, the write phase-locked ~~peep~~ loop circuit comprising a second VCO that oscillates to generate an oscillating clock, a selector for selecting one of a synchronization signal derived from the prerecorded signal and a divisional signal frequency-divided from the read clock at the same frequency as the synchronization signal, and a second phase comparator for comparing a phase or the selected one of the synchronization signal and the divisional signal with a phase of a clock signal derived from the oscillating clock of the second VCO so as to control the second VCO

based on phase-comparison between the selected signal and the clock signal to thereby generate the write clock phase-locked to the selected signal;

a detecting circuit that detects the phase of each frame of the read signal derived from the previous information;

a generating circuit that generates a write signal representative of the new information in synchronization to the oscillating clock generated from the second VCO; and

a control circuit that operates before starting the writing of the new information subsequent to the end of the previous information for controlling the read phase-locked ~~peop~~ loop circuit to conduct the reading of a part of the previous information including the end thereof in synchronization to the read clock generated by the read phase-locked ~~peop~~ loop circuit while controlling the selector of the write phase-locked ~~peop~~ loop circuit to select the divisional signal of the read clock for synchronizing the oscillating clock of the second VCO with the read clock, and then operates when the reading of the previous information reaches the end for controlling the generating circuit to generate the write signal in matching with the phase of the last frame of the read signal detected at the end of the previous information to thereby start the writing of the new information in continuation from the end of the previous information and then controlling the selector of the write phase-locked ~~peop~~ loop circuit to select the synchronization signal for synchronization of the write clock.

20. (Currently Amended) The apparatus according to claim 19, further comprising a divider for dividing the oscillating clock fed from the second VCO by a variable division ratio to produce the clock signal fed to the second phase comparator, a third phase

comparator for comparing a phase of each frame of the write signal with a phase of the synchronization signal derived from the pre-recorded signal to determine a phase difference between the write signal and the synchronization signal, and an adjuster operative after the selector of the write phase-locked ~~peop~~ loop circuit is switched from the divisional signal of the read clock to the synchronization signal of the prerecorded signal for adjusting the variable division ratio of the divider so as to gradually absorb the phase difference.

21. (Currently Amended) The apparatus according to claim 19, wherein the control circuit operates when switching the selector of the write phase-locked ~~peop~~ loop circuit from the divisional signal of the read clock to the sync clock of the pre-recorded signal, for resetting a phase of the clock signal fed to the second phase comparator in matching with a phase of the synchronization signal derived from the pre-recorded signal.